AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) Device for processing data, comprising:

a processor for executing program routines, and a memory for storing program routines to be executed by said processor, where

at least a part of said memory is arranged as a protected part from which data can be read but which is protected against being written into, where said protected part is arranged such that a mechanism is provided such that after data is initially stored in said protected part, any subsequent writing of data into said protected part is irreversibly blocked, and

said processor is arranged to necessarily execute a program routine stored in said protected part of said memory upon start-up.

2. (Previously Presented) Device according to claim 1, wherein said processor stores permanent start addresses that are necessarily called upon start-up of said processor, where at least one of said start addresses points to said protected part of said memory.

3. (Previously Presented) Device according to claim 1, wherein said protected part of said memory is a first part, and said memory further comprises a second part into which data can be written, where the program routine from said protected part executed

by said processor upon start-up comprises checking for changes in at least a part of the data contained in said second part.

4. (Previously Presented) Device according to claim 3, wherein said program routine from said protected part executed by said processor upon start-up comprises calculating a characteristic parameter for data being checked for changes, and comparing said characteristic parameter with a value stored in said second part of said memory at the time of writing said data being checked for changes into said second part of said memory.

5. (Original) Device according to claim 4, wherein said characteristic parameter is a check sum.

6. (Previously Presented) Device according to claims 1, wherein said memory comprises a plurality of memory devices, one of which comprises said protected part, and the rest of which are arranged such that data may be written into them.

7. (Cancelled)

8. (Currently Amended) Device according to claim ~~7~~ 1, wherein said protected area is arranged such that the process for storing data therein comprises:

writing data into said protected part via a write line, and

sending a signal to said protected part in response to which said write line is permanently interrupted.

9. (Original) Device according to claim 8, wherein said write line is a fusable link.

10. (Previously Presented) Device according to claim 1, wherein said memory comprises a finite state machine, said finite state machine defining a state which protects said protected part from being written into.

11. (Previously Presented) Device according to claim 1, wherein said memory comprise one or more of an EEPROM, a flash memory device, and a flash memory device emulating an EEPROM.

12. (Previously Presented) Device according to claim 1, wherein said memory comprises a memory chip having electrical contacts for being connected with a circuit board that are arranged such that said electrical contacts are covered by said memory chip when said memory chip is mounted on said circuit board.

13. (Previously Presented) Device according to claim 12, wherein said electrical contacts are provided in a ball-grid-array.

14. (Previously Presented) Communication device comprising a device for processing data according to claim 1.

15. (Original) Communication device according to claim 14, wherein said communication device is a mobile telephone.

16. (Original) Communication device according to claim 14, wherein said communication device is a bluetooth communication device.

17. (Previously Presented) Method for controlling a data processing device having a processor for executing program routines and a memory for storing program routines to be executed by said processor, comprising:

arranging at least a part of said memory as a protected part from which data can be read but which is protected against being written into;

after data is initially stored in said protected part, irreversibly blocking any subsequent writing of data into said protected part; and

said processor necessarily executing a program routine stored in said protected part of said memory upon start-up.

18. (Original) Method according to claim 17, wherein said processor stores permanent start addresses that are necessarily called upon start-up of said processor, where at least one of said start addresses points to said protected part of said memory.

19. (Previously Presented) Method according to claim 17, wherein said protected part of said memory is a first part, and said memory further comprises a second part into which data can be written, where the program routine from said protected part executed by said processor upon start-up comprises checking for changes in at least a part of the data contained in said second part.

20. (Original) Method according to claim 19, wherein said program routine from said protected part executed by said processor upon start-up comprises calculating a characteristic parameter for data being checked for changes, and comparing said characteristic parameter with a value stored in said second part of said memory at the time of writing said data being checked for changes into said second part of said memory.

21. (Original) Method according to claim 20, wherein said characteristic parameter is a check sum.

22. (Previously Presented) Method according to claim 17, wherein said memory comprises a plurality of memory devices, one of which comprises said protected part, and the rest of which are arranged such that data may be written into them.

23. (Cancelled)

24. (Currently Amended) Method according to claim ~~23~~ 17, wherein said protected area is arranged such that the process for storing data therein comprises:

writing data into said protected part via a write line, and

sending a signal to said protected part in response to which said write line is permanently interrupted.

25. (Original) Method according to claim 24, wherein said write line is a fusable link.

26. (Previously Presented) Method according to claim 17, wherein said memory comprises a finite state machine, said finite state machine defining a state which protects said protected part from being written into.

27. (Previously Presented) Method according to claim 17, wherein said memory comprises one or more of an EEPROM, a flash memory device, and a flash memory device emulating an EEPROM.

28. (Previously Presented) Method according to claim 17, wherein said memory comprises a memory chip having electrical contacts for being connected with a circuit board that are arranged such that said electrical contacts are covered by said memory chip when said memory chip is mounted on said circuit board.

29. (Original) Method according to claim 28, wherein said electrical contacts are provided in a ball-grid-array.

30. (Previously Presented) A medium readable by a data processing device, having a program recorded thereon, where the program is to make the data processing device execute the method of claim 17.